1. A system to transmit and receive information by encoding and decoding discreet data into and from analog waveforms, said system comprising:

a) a first microcontroller adapted to receive a digital data stream, said microcontroller being arranged to manipulate said digital data stream to frame said digital data stream to provide data bit assembly in accordance with a desired protocol, to provide for addition of miscellaneous flag data, and to provide for the addition of error correction data, and also arranged to output said manipulated data as a manipulated digital data stream;

b) a continuously variable slope delta demodulator (CVSD) to receive said manipulated digital data stream and to convert said manipulated digital stream to an analog signal;

c) a continuously variable slope delta (CVSD) modulator arranged to receive the analog output signal from said CVSD demodulator, and to output a digital data stream;

d) a second microprocessor arranged to receive said digital data stream from said CVSD modulator and to unframe said digital data stream, perform error checking and corrections, perform data bit deinterleaving according to said desired protocol, and output a recovered digital data stream corresponding to said initial digital data stream.

2. A method of transmitting and receiving information by encoding and decoding discreet data into and from analog waveforms, said method comprising:

a) receiving a digital data stream, and then manipulating said digital data stream to frame said digital data stream to provide data bit assembly in accordance with a desired protocol, provide for addition of miscellaneous flag data, and provide for the addition of error correction data, and also arranged to output said manipulated data as a manipulated digital data stream;

b) utilizing a a continuously variable slope delta demodulator (CVSD) to receive said manipulated digital data stream and to convert said manipulated digital stream to an analog output signal;

c) utilizing a continuously variable slope delta (CVSD) modulator to receive the analog output signal from said CVSD demodulator, and to output a digital data stream;

d) receiving said digital data stream from said CVSD modulator and unframing said digital data stream, performing error checking and corrections, performing data bit deinterleaving according to said desired protocol, and providing an output of a recovered digital data stream corresponding to said digital data stream.

3. The apparatus as recited in claim 1, wherein:

a) there is a universal asynchronous receiver/transmitter to receive the digital data stream and convert the digital data stream to a parallel data stream output which is transmitted to said first microcontroller;

b) a second universal asynchronous receiver/transmitter to receive a parallel output from said first microcontroller and transmit said manipulated digital data stream to said continuously variable slope delta demodulator;

c) a band pass filter to receive the analog signal from the said continuously variable slope delta demodulator;

d) a variable gain unit to receive an output from the band pass filter;

e) a blocking capacitor to receive an output from the variable gain unit and transmit an output to a transmitter to transmit the analog signal output from the first universal asynchronous receiver/transmitter.